



**CLEAN VERSION OF SPECIFICATION PARAGRAPH  
BEGINNING ON PAGE 9, LINE 26, ENDING ON PAGE 10, LINE 3**

**CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL  
TRANSISTOR AND TRENCH CAPACITOR**

Applicant: Wendell P. Noble et al.

Serial No.: 09/551,027

202C  
C2

Each memory cell is constructed in a similar manner. Thus, only memory cell 202C is described herein in detail. Memory cell 202C includes pillar 204 of single crystal semiconductor material, e.g., silicon, that is divided into second source/drain region 206, body region 208, and first source/drain region 210 to form access transistor 211. Pillar 204 extends vertically outward from substrate 212 of, for example, p- silicon. Second source/drain region 206 and first source/drain region 210 each comprise, for example, n + silicon and body region 208 comprises p- silicon.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH  
BEGINNING ON PAGE 10, LINE 12, ENDING ON PAGE 10, LINE 21**

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Sub C3  
Memory cell 202C also includes storage capacitor 219 for storing data in the cell. A first plate of capacitor 219 for memory cell 202C is integral with first source/drain region 210 of access transistor 211. Thus, memory cell 202C may be more easily realizable when compared to conventional vertical transistors since there is no need for a contact between first source/drain region 210 and capacitor 219. Second plate 220 of capacitor 219 is common to all of the capacitors of array 200. Second plate 220 comprises a mesh or grid of n+ poly-silicon formed in deep trenches that surrounds at least a portion of first source/drain region 210 of each pillar 204A through 204D. Second plate 220 is grounded by contact with substrate 212 underneath the trenches. Second plate 220 is separated first source/drain region 210 by gate oxide 222.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH  
BEGINNING ON PAGE 11, LINE 1, ENDING ON PAGE 11, LINE 7**

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C<sup>4</sup> Figure 4 is a schematic diagram that illustrates an effective circuit diagram for the embodiment of Figures 2 and 3. It is noted that storage capacitor 219 formed by first source/drain region 210 and second plate 220 is depicted as four separate capacitors. This represents that the first plate 220 surrounds second source/drain region 210 which increases the charge storage capacitance and stored charge for the memory cell. It is also noted that second plate 220 is maintained at a constant potential, e.g., ground potential.

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